A Low-power 435-MHz SOI CMOS LNA and Mixer

Ertan Zencir[1], Numan S. Dogan[1] and Ercument Arvas[2]

[1]North Carolina A&T State University, Electrical Engineering Dept., Greensboro, NC, 27411
[2]Syracuse University, EECS Department, Syracuse, NY, 13244

Abstract — **A low-power 435-MHz single-ended low-noise amplifier and a double-balanced mixer was implemented in a 0.35-μm Silicon On Insulator (SOI) CMOS process. The single-ended LNA has a measured noise figure of 2.91 dB, and the mixer has an input third-order intercept point of +20 dBm. Total power dissipation of the LNA and mixer is 24 mW from a 2.5-V supply. This is the first LNA-mixer pair implemented at 435 MHz using an SOI CMOS process.**

I. INTRODUCTION

Although there has been improvements in bulk CMOS processes for analog applications, analog circuits implemented on bulk CMOS are susceptible to cross-talk, substrate noise, and Q factor degradation of integrated inductors due to the low-resistivity substrates [1]. Digital, mixed-signal, and RF integrated circuit designers have shown interest in the SOI CMOS process for low-power and high-speed applications. However, there is not a broad literature of SOI CMOS analog, mixed-signal, or RF integrated circuit implementations covering different frequency ranges or applications.

Fig. 1 shows the cross-section of a typical SOI CMOS structure. A bulk CMOS transistor and the SOI CMOS transistor have many features in common with the additional feature of an insulating layer under the thin active layer. This isolation layer eliminates many of the problems associated with the active device-substrate interactions. Substrate of the SOI CMOS process used for this design is a highly resistive substrate as opposed to low-resistivity substrates in bulk CMOS. The active silicon layer is isolated on all sides. To the right and left of the active silicon layer are the shallow trench isolation (STI), which is similar to the STI isolation used in bulk CMOS. Gate oxide thickness is comparable to the thickness in a typical CMOS process.

High-resistivity SOI substrate suppresses the losses from bonding pads, integrated spiral inductors and noise coupled through the substrate. Reduced substrate noise coupling makes SOI CMOS particularly attractive for full integration of RF and digital circuits on the same substrate [1].

High-substrate resistivity and buried oxide layer provides isolation to decrease substrate noise injected by noisy digital circuits into sensitive analog parts. High resistivity bulk in the SOI CMOS also offers the possibility of improving passive components Q-factor.

SOI CMOS active devices show high-speed performance even at low supply voltages (~ 1V). Lower threshold voltages of SOI CMOS active devices makes low power designs possible. In SOI CMOS devices, junction capacitance is merely the buried oxide capacitance, which may be 4 to 7 times smaller than in bulk CMOS. Poly-to-substrate and metal-to-substrate capacitances are also lower. SOI CMOS is also highly attractive for deep space communication transceivers since it is a radiation-hard process. SOI CMOS transistors suffer from the transconductance nonlinearity like the bulk CMOS transistors but it is not effected by the voltage-dependency of drain capacitance due to the presence of the buried oxide layer.

Performance of passive devices in SOI CMOS process is better than the devices in bulk CMOS. There have been reports on integrated spiral inductors built in SOI CMOS processes having higher quality factors and higher self-resonance frequencies than their bulk CMOS counterparts [2]. Examples demonstrating the performance of high-Q SOI inductors can be found in [3].

Although there are some published SOI CMOS LNA and mixer works in the GHz range [4]-[6], none have been reported so far at UHF frequencies. In this work, a low-power 435-MHz SOI CMOS LNA and mixer design is realized and the measured results are presented. The paper is organized as follows. The LNA and mixer design is introduced in section 2. Measurement results are presented in section 3. Section 4 concludes the paper.

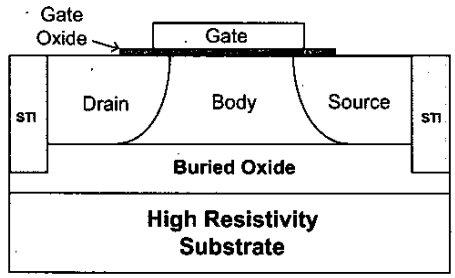

Fig. 1. Cross-section of an SOI CMOS structure

0-7803-7695-1/03/$17.00 © 2003 IEEE

II. The Design of the LNA And the Mixer

The low-noise amplifier is a single-ended one with source degeneration. The LNA schematic and the element values are shown in Fig. 2. Single-ended topology is adopted due to the difficulty of finding low-loss balun transformers at UHF. Balun transformers available at UHF decrease the gain and increase the noise figure by more than 1 dB. The high isolation of the buried oxide layer makes it possible to design high performance single ended receiver blocks since the substrate noise is significantly suppressed. The inductor L_s provides a real part to the input impedance at the gate of M1. That real part which is in the order of 100-150Ω is reduced to lower values due to the presence of the parasitic capacitance impressed by the pads and ESD protection diodes (represented by C_p in Fig. 2). The real part and the imaginary part of the input impedance is then matched to 50 Ω through an off-chip L-matching section (L_m and C_m).

The equal size transistors M1 and M2 constitute a cascode configuration that lowers the Miller capacitance preventing the input impedance degradation. Cascode configuration also provides increased input-output isolation. Drain inductor L_d is adjusted such that it will resonate with the total parasitic drain capacitance of M2 at 435 MHz. Transistors are chosen as 350-μm wide although this is not the noise optimum width at 435 MHz according to [7]. Optimum width is not selected since low overdrive voltage is not acceptable for proper biasing and operation of the LNA. On-chip p-well resistor R_b provides the bias voltage for the input transistor M1. Bodies are tied to the transistor sources which offer small threshold voltage levels (~ 0.65 V). Use of multifinger gates in the layout results in a significant decrease in the gate electrode resistance which directly affects the RF performance.

The mixer schematic is shown in Fig.3. Table I shows the element values of the mixer. The mixer has a double-balanced topology, which consumes twice the current of a single-balanced mixer. However, the double-balanced topology does not have the disadvantage of local oscillator feedthrough inherent in single-balanced topology. The mixer downconverts the RF signal at 435 MHz to an intermediate frequency of 2 MHz. Devices N1 and N2 are used as transconductance amplifier and the transistor pairs N3-N4 and N5-N6 make up the mixing cell. Gates of the mixer transistors N1-N6 are biased through on-chip polysilicon resistors. An on-chip constant-g_m bias circuit, which offers stability against temperature and supply voltage variations is realized by PMOS transistors P1-P4 and NMOS transistors N7-N14. The value of this current is controlled by the off-chip resistor R_v. NMOS transistors N13-N14 and the resistor R_{st} are for the startup of the constant-g_m bias circuit. The mixer load is realized by resistors R_L. LO source power is 0 dBm. The single-ended LNA output will be coupled to one of the mixer inputs and the other mixer input will be shorted to ground through a high value capacitor in the full receiver implementation phase. By doing so, advantages of having a differential topology and a better noise performance of the LNA could be combined together without the need for any balun transformers. All the simulations of the LNA and the mixer were done using SpectreRF.

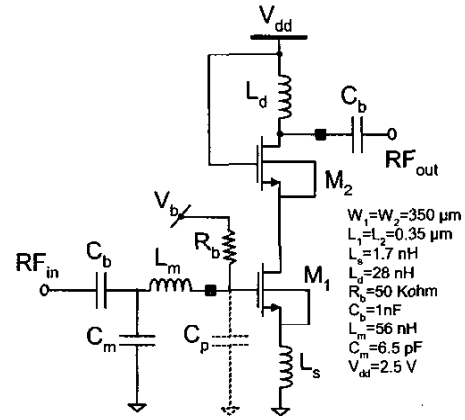

Fig. 2. The single-ended LNA circuit.

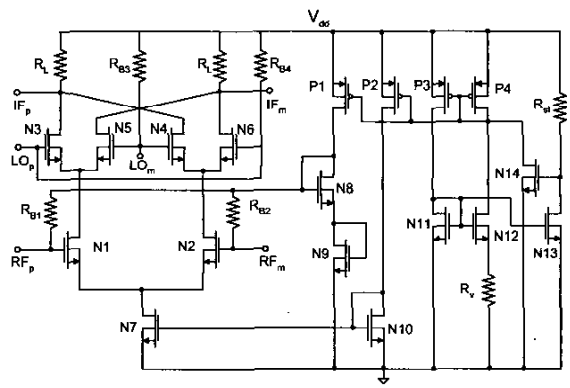

Fig. 3. Double-balanced mixer circuit.

TABLE I.
MIXER ELEMENTS

N1,N2	120/0.8 μm	P1	60/1.55 μm
N3-N6	50/0.35 μm	P2-P4	120/1.55 μm
N7	350/1.2 μm	R_{B1},R_{B2}	50 kΩ
N8,N9	100/1.5 μm	R_{B3}	30 kΩ
N10	30/1.2 μm	R_v	650 Ω
N11,N13	30/0.5 μm	R_{st}	20 kΩ
N12	240/0.5 μm	R_L	500 Ω
N14	45/1.55 μm	V_{dd}	2.5 V

III. MEASUREMENT RESULTS

Figures 4 and 5 show the measured small-signal gain, input reflection and the input-output isolation of the LNA. The LNA provides a small-signal gain of 17.5 dB. Input return loss is 24 dB and the input-output (reverse) isolation is 26 dB. The noise figure as a function of frequency is shown in Fig. 6. The noise figure at 435 MHz is 2.91 dB. Total power dissipation of the LNA is 12.5 mW from a 2.5-V supply. Sweeping the input power of the LNA and measuring the small-signal gain, it was found out that the 1-dB compression point is at -13.7 dBm. The two-tone analysis is done by applying two RF signals at the input of the LNA at the frequencies of 435 MHz and 440 MHz and sweeping their power. Figure 7 shows the two-tone characteristics of the LNA. Input IP3 point of the LNA is at -1 dBm.

Table II summarizes the mixer measurement results for conversion gain, noise figure and port-to-port isolations. Very good port-to-port isolation is obtained with a typical mixer noise figure performance. Fig. 8 shows the measured output IF power (at 2 MHz) as a function of the RF signal power (at 435MHz) with an LO frequency of 437 MHz and LO power of 0 dBm. Output power deviates by 1 dB from the linear input-output relation when the RF input power is 4 dBm. Two-tone characteristic is obtained by applying two RF signals at 435 MHz and 436 MHz combined with a 3-dB coupler. LO power is set to 0 dBm and the input RF signal power levels are swept simultaneously and measured output fundamental and third-order intermodulation component power levels are shown in Fig. 9. An extrapolation of the linear sections of these two curves reveal an input IP3 of +20 dBm. Total power dissipation of the mixer is 11.5 mW from a 2.5-V supply.

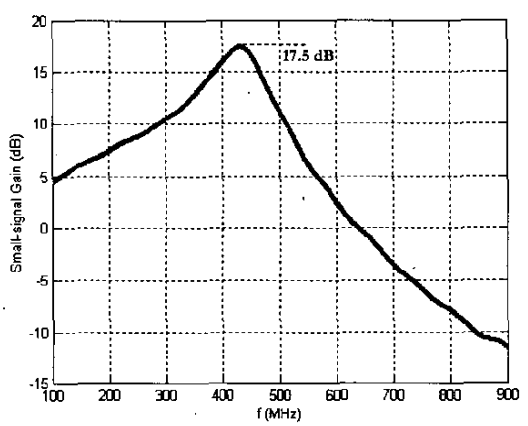

Fig. 4. Small-signal gain of the LNA

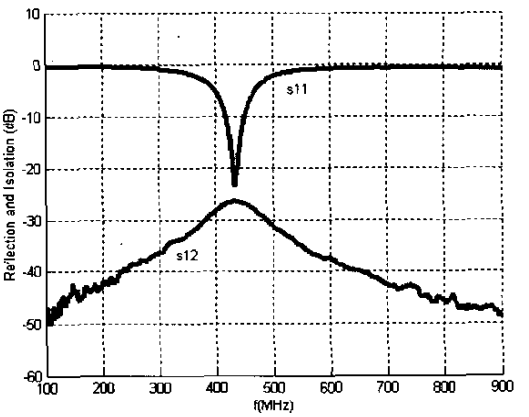

Fig. 5. Input reflection and reverse isolation of the LNA

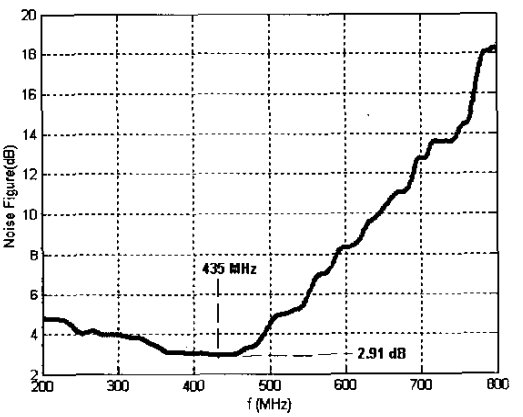

Fig. 6. Noise figure of the LNA

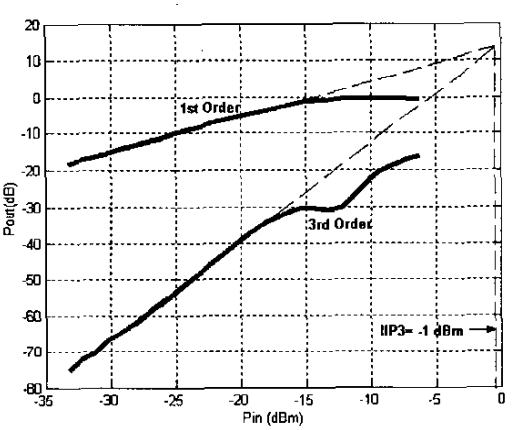

Fig. 7. Two-tone characteristics of the LNA

TABLE II.
MIXER MEASURED PERFORMANCE

Conversion Gain	5.5 dB
LO-RF Isolation	44 dB
LO-IF Isolation	49 dB
RF-IF Isolation	47 dB
Noise Figure @ 2-MHz IF	13 dB
LO power @ 437 MHz	0 dBm
Supply Voltage	2.5 V
Power dissipation	11.5 mW

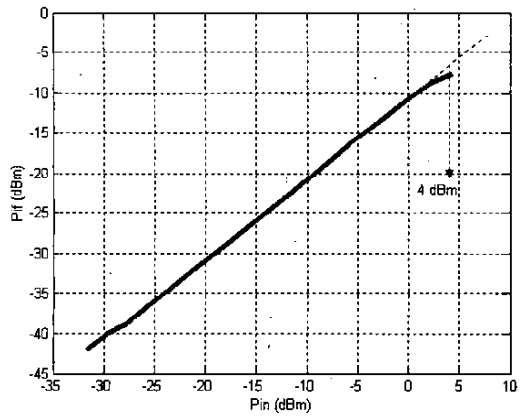

Fig. 8. Mixer IF output power versus RF input power

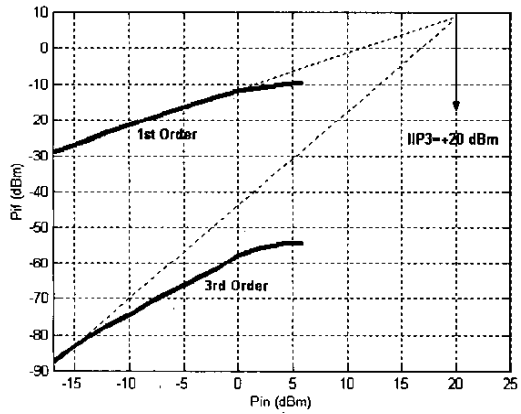

Fig. 9. Two-tone characteristics of the mixer

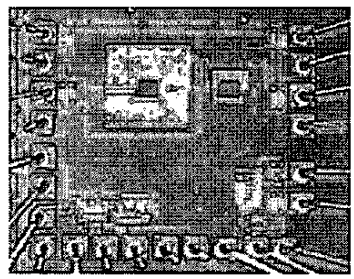

Fig. 10. Microphotograph of the SOI LNA and mixer chip

Total power dissipation of the LNA and mixer is 24 mW. Microphotograph of the wirebonded LNA-mixer chip is shown in Fig. 10. Input and output pads are ESD protected with the reverse-biased junction diodes. The die area occupied by the LNA and the mixer are 0.6 mm x1.4 mm and 0.6 mm x 0.9 mm, respectively.

IV. CONCLUSION

A low-power LNA-mixer pair has been implemented using a 0.35-μm SOI CMOS process. Measurement results show that designing RF building blocks is feasible in SOI CMOS with good performance. This and other arising RFIC works done by using SOI CMOS technology offers promise for future realization of receiver systems such as GSM, GPS and Bluetooth using SOI CMOS. This work is a full demonstration of the possible future tracks in the analog IC design area that will use SOI CMOS.

ACKNOWLEDGEMENTS

This work is supported by NASA through a grant number NAG3-2584. The authors would like to thank Gene Fujikawa of NASA Glen Research Center; Mohammed Mojarradi, Norman Lay and Martin Herman of Jet Propulsion Laboratory, California Institute of Technology for their support and collaboration.

REFERENCES

[1] A. O. Adan, T. Yoshimasu, S. Shitara, N. Tanba, and M. Fukumi, "Linearity and low-noise performance of SOI MOSFET's for RF applications," *IEEE Transactions on Electron Devices*, vol. 49, pp.881-888, May 2002.

[2] H. Jin, and C. A. T. Salama, "A 1-V, 1.9-GHz CDMA, CMOS on SOI, low noise amplifier," *IEEE International SOI Conference*, pp. 102-103, Oct. 2000.

[3] E. Zencir, N. S. Dogan, and E. Arvas, "Modeling and performance of spiral inductors in SOI CMOS technology," *IEEE Canadian Conference on Electrical and Computer Engineering*, May 2002, pp. 408-411

[4] Wei Jin, Weidong Liu, Chaohe Hai, Chan, P.C.H., and Chenming Hu, "Noise modeling and characterization for 1.5-V 1.8-GHz SOI low-noise amplifier," *IEEE Transactions on Electron Devices*, vol. 48, pp. 803-809, April 2001.

[5] Wei Jin, Chan, P.C.H., and Chaohe Hai, "1.5-V 1.8-GHz SOI low noise amplifiers for PCS receivers," *IEEE International SOI Conference*, pp. 16-17, 1999.

[6] C. A. T. Salama, and Ye Song, "A 1 V, 1.9 GHz, low distortion dual-gate CMOS on SOI mixer," *IEEE International SOI Conference*, pp. 104-105, 2000.

[7] T. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Cambridge University Press, 1998.